1996 Paper 5 Question 1

Processor Architecture

What is a *branch delay slot* and why does it arise? [7 marks]

How can branch delays be avoided? [7 marks]

If a processor exhibited one branch delay slot how would you reorder (and possibly modify) the instructions in the following loop to gain a performance advantage?

```
loop
        ldr r2,r3,#4     % r2=load(r3), r3=r3+4
        add r4,r4,r2     % r4=r4+r2
        add r1,r1,#1     % r1=r1+1
        cmp r1,#10       % compare r1 with constant 10
        bne loop         % branch if not equal to loop
```

[6 marks]