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Design and Implementation of an Autostereoscopic Camera System

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Abstract

An autostereoscopic display provides the viewer with a three-dimensional image without the need for special glasses, and allows the user to "look around" objects in the image by moving the head left-right. The time-multiplexed autostereo display developed at the University of Cambridge has been in operation since late 1991.

An autostereoscopic camera system has been designed and implemented. It is capable of taking video input from up to sixteen cameras, and multiplexing these into a video output stream with a pixel rate an order of magnitude faster than the individual input streams. Testing of the system with eight cameras and a Cambridge Autostereo Display has produced excellent live autostereoscopic video.

This report describes the design of this camera system which has been successfully implemented and demonstrated. Problems which arose during this process are discussed, and a comparison with similar systems made.

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1. Introduction

An autostereoscopic display provides the viewer with a three-dimensional image without the need for special glasses, and allows the user to "look around" objects in the image by moving left-right.

The time-multiplexed autostereo display developed at the University of Cambridge has been in operation since late 1991 [Trav90, TrLa91, LTCM92, TLMD95, MDTL96]. Images have been supplied to this display from a standard framestore in an IBM PC, allowing experiments with still pictures and interactive computer-generated images. A real-time autostereo camera system is now in operation. This takes multiple video signals from an array of standard video cameras, and multiplexes them together in real time to produce a single autostereo video stream for the autostereo display.

This report describes the design of this camera system which has been successfully implemented and demonstrated. Problems which arose during this process are discussed, and a comparison with similar systems made.

2. The autostereo display

An autostereoscopic display provides the viewer with a true three dimensional image, with stereo parallax and the ability to "look-around" objects in the image by moving her or his head. There is no need for the viewer to wear special glasses or other head gear, and several viewers can simultaneously see the autostereo image from their individual viewpoints.

Various methods have been proposed for an autostereoscopic display, including parallax barriers [Eich93], spinning plane devices [BlSH94], lenticular screens [ITYK92] and dynamic holograms [Bent87]. The Cambridge autostereo display [MDTL96] utilises a field sequential (time-multiplexed) scheme where light emitted from a conventional array of pixels (in this case a high speed CRT) is directionally modulated by a dynamic optical system so that each field in the sequence is visible only over a narrow view angle in front of the display.

These views are arranged laterally (Figure 1) so that each of the user's eyes sees a different image. The images are presented sequentially sufficiently quickly that each individual view is refreshed at normal TV

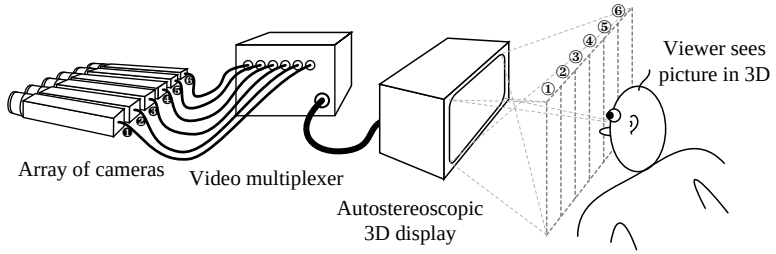

Figure 1: a six view autostereo display produces a different image on the screen for each of the six zones in space. Because his eyes are in different zones, the viewer sees one image with his left eye and a different image with his right eye, thus perceiving a 3D picture. The video multiplexer described in this report ensures that the image from each of the six cameras is visible in the appropriate zone.

field rate. If the user moves her head, she will see a different pair of images, providing the look-around capability. Appropriate images must therefore be displayed on the CRT in synchronisation with the different view directions of the dynamic modulator.

Each separate view angle of the modulator requires a different perspective 2D image of the subject. The more views there are, the finer the granularity of the autostereoscopic effect as the viewer moves her head, and the closer the approximation to a holographic display — at least in the horizontal direction.

Several displays of this design are in operation, with an 8" x 6" screen (10" diagonal) capable of displaying 16 views at 640×240 pixels resolution, or 8 views at 640×480 pixels resolution. Both modes of operation refresh the complete stereoscopic image at 50Hz, with overall field rates of $(16+1) \times 50$Hz and $(8+1) \times 50$Hz respectively. The current limits on refresh rate are: pixel rate 150MHz, line rate 150kHz, field rate 2000Hz. Modifications are underway to increase the first two by 30–40%. A more detailed description can be found in [LTCM92].

3. Autostereo display video format

The autostereo display accepts interlaced or non-interlaced video at a frame rate eight or sixteen times greater than conventional TV video. The

video stream consists of a sequence of fields, one for each view in turn, progressing from left to right. A final blank view is required when interlacing with an even number of visible views (as detailed later) [MTLC92]. In addition to the video signal, a composite sync signal is required on an additional input. Alternatively separate horizontal and vertical sync signals may be provided.

The only necessary non-standard input is the Z-sync signal (the so called *azimuth* sync signal). This is a single short pulse during the final field of an autostereo set of views. The pulse indicates to the display that the next field is the odd field for view one (the leftmost view). In non-interlaced operation it simply indicates that the next field is for view one. The Z-sync signal ensures that the dynamic directional modulation is correct for each field displayed on the CRT.

4. The camera array

Video input for the autostereo display is sourced from an array of cameras. As many cameras are required as there are visible views on the display. They are arranged in a horizontal row spaced a suitable distance apart and mounted so that they can be easily aligned (Figure 2(b)).

For use at close distances (3–6'/1–2m) the centre to centre separation of the cameras is on the order of 1" (25mm) for an eight camera system. This necessitates the use of miniature cameras. Several such cameras were considered and the Sony XC-999P finally chosen as a trade-off between cost and quality of image. It also has the desirable feature of being able to accept an external synchronising signal.

The cameras can be mounted in two ways: either radially about some central point (this point being at or near the objects that are to be viewed) or parallel to one another [DoLa93, CGDS93]. In the former case (the *radial* case) the central point will appear in the plane of the autostereo display's screen. However, objects at some distance in front of or behind this point will seem distorted and hard to fuse stereoscopically (Figure 2(a)), as will objects near the left and right edges of the screen.

The second, *parallel* case is the correct one (Figure 2(b)). Because all images are displayed on the same flat screen, all of the cameras' CCD

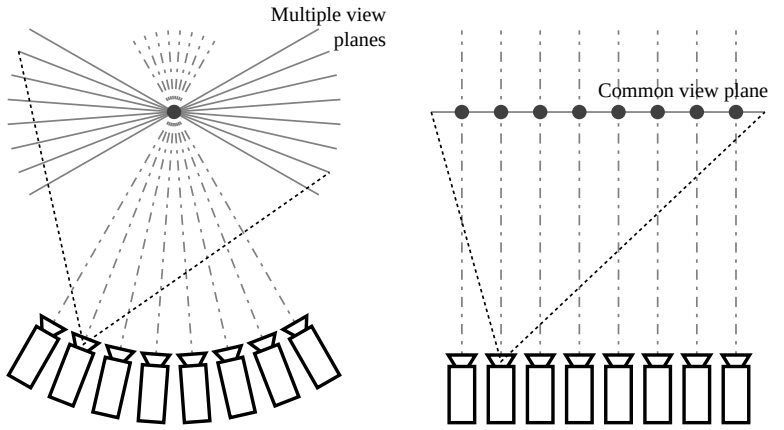

Figure 2: (a) shows the incorrect radial arrangement of cameras. This is incorrect because the multiple view planes from the different cameras are all displayed on a single screen plane, causing perspective distortion of the 3D picture. (b) shows the correct parallel arrangement of cameras. The common view plane is displayed on the single screen and the resulting 3D effect is good.

arrays should lie in the same plane to prevent distortions. With no further modifications, objects at infinity would appear to lie in the plane of the autostereo display's screen, with all other objects appearing to lie in front of the screen. This is undesirable in normal operation because the usable volume of the display lies three quarters behind the screen and only one quarter in front. Various techniques can be used to make a selectable distance from the cameras appear in the screen plane [CGDS93].

Because of its simplicity, the *radial* arrangement was used for testing of the system. The depth of view was limited to prevent viewer problems.

Each camera in the array is connected to the camera system via a single cable which supplies power and synchronising signals, and the camera video output. The cameras are operated in 50Hz PAL format, and Y/C output is used to get the best resolution.

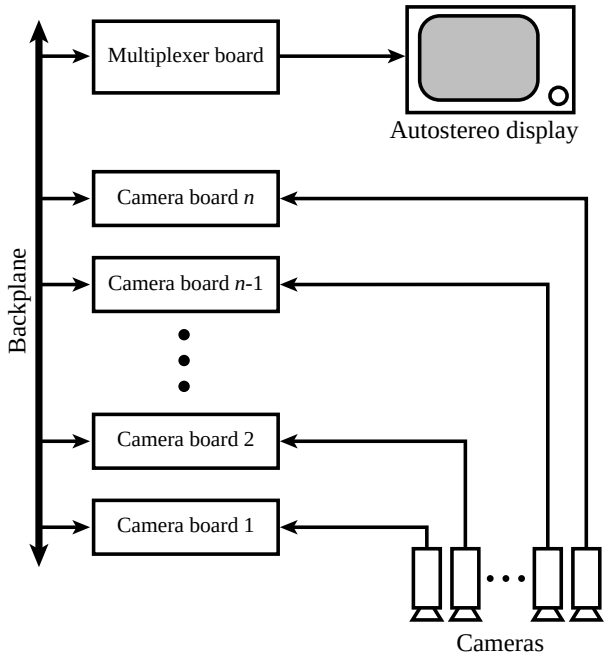

Figure 3: an overview of the autostereo camera system. Each of a set of cameras feeds a camera board. These are multiplexed together across a backplane, and the resulting output fed to the autostereo display.

5. Overview of the camera system

The input streams from the multiple cameras must be field-multiplexed together for output to the autostereo display, in the correct order with odd/even field polarity maintained. Figure 3 gives an overview of the system.

A single circuit board (the *multiplexer* board) contains all of the components required for mutiplexing the digital data stream from the individual camera boards, and a potentially very simple circuit board (the *camera* board) contains the components necessary for digitising and processing an individual camera signal. An identical camera board is

required for each camera in the camera array. The display is capable of showing up to sixteen views, and so the camera system is able to accommodate up to sixteen cameras.

The various boards are connected together by a backplane. Power is supplied to all boards and cameras from a standard power supply unit.

The parallel input/serial output nature of the device and the need to maintain field polarity means that each camera board requires sufficient on-board memory to store at least three fields. An ability to crop and downsize the video picture is also desirable to give flexibility.

The multiplexer board must access each camera board's memory in the correct sequence to produce the autostereo video stream. In addition, this board contains all of the overall control circuitry, the sync signal generators for the autostereo display, and the sync signal generator for globally synchronising the cameras together.

6. The camera boards

Each camera board (figure 4) consists of four groups of components to perform the following four tasks:

Digitising, decoding and (optionally) resizing of the video signal.

Storing the resulting digital video data.

Buffering the stored data onto a backplane and from there to the multiplexer board.

Controlling the above three groups.

A Philips chip set [Phil93] was chosen to perform the first stage, because it has a particularly simple electrical interface, and there was already experience in using the set within the Laboratory. This chip set consists of five integrated circuits:

A pair of A/D converters: the TDA8708 for luminance (Y) or composite video, and the TDA8709 for chrominance (C) for use with a Y/C input.

A video signal decoder (SAA7191)

Its associated clock generation chip (SAA7197).

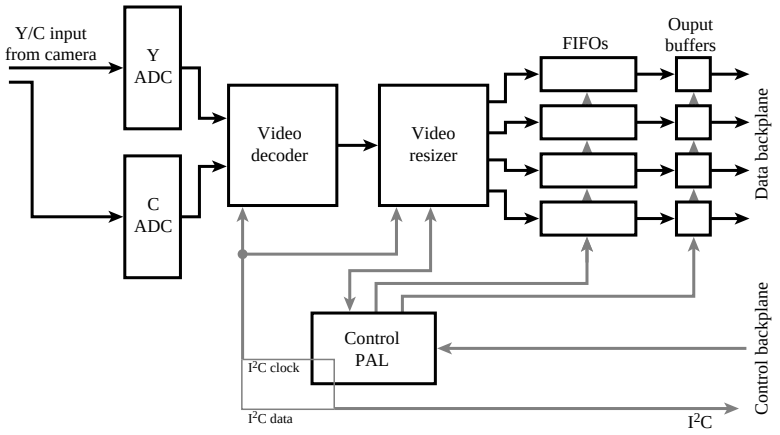

Figure 4: block diagram of the camera board.

A picture resizer chip (SAA7186) which can arbitrarily downsize and crop the video picture, and produce output in a variety of formats.

Both SAA7191 and SAA7186 are programmed via Phillips I^{2}C (inter integrated circuit) bus [Phil93]. The use of these two chips on each camera board means that the I^{2}C bus must be gated between the I^{2}C master and each instance of the two chips. This gating is discussed fully in the following section.

On output from the SAA7186 resizer, the video data must be stored pending output to the multiplexer board and, from there, to the autostereo display. FIFOs were chosen as the storage medium in the prototype because of the simplicity of controlling input and output from them. NEC's µPD42280 was selected because of its size (2 Mbit arranged 8 wide, hence 256kB) and high speed. Four of these are required in parallel because the SAA7186 uses a 32-bit wide output port in some output formats. For example: the monochrome mode around which the system is designed uses these 32 bits as four 8-bit adjacent pixel values.

Output from the FIFOs is re-timed by a bank of 32 D-type flip-flops and from there to tri-state buffers which drive the data over the backplane. The

FIFOs are specified to run at up to 33MHz over the full temperature range, but trials have had the output side running in bursts at 36MHz with no trouble.

Overall control of the camera board is provided by an AMD Mach-110 PAL (programmable array logic) in conjunction with various signals supplied by the multiplexer board. The PAL mediates data transfer from the SAA7186 resizer to the FIFOs and from these to the backplane, gates the various signals from the multiplexer board, and provides the means of gating the I^{2}C bus.

7. Gating the I^{2}C bus

Four of the control lines from the multiplexer board select which of the camera boards is currently active, that is: which camera board is currently sending video data to the D/A converter on the multiplexer board. These four selection lines, in conjunction with four switches on the camera board, are decoded by the camera board's PAL to provide a gating control for the global *active* signal from the multiplexer board. This *active* signal controls transfer of video data from camera board to multiplexer board. When inverted it is the video blanking signal for the D/A converter.

Provision is made on the multiplexer board for the I^{2}C master to override the values on the four selection lines. This mechanism permits the use of the same PAL-generated gating signal to gate the I^{2}C bus. Four separate selection lines could have been used for gating the I^{2}C bus, at the cost of requiring four extra control lines on the backplane.

The I^{2}C bus is not designed to be gated. It is made up of two bi-directional lines: one data and one clock. Each device on the I^{2}C bus has to have a unique address to allow multiple devices to be connected on a single bus [Phil93]. The SAA7191 and SAA7186 are provided with only two unique addresses each (hardware selectable via a pin), thus only two of each could be attached to an ungated bus.

Two solutions are possible: (1) to gate one of the lines bi-directionally, perhaps using a balanced pair of FETs; or (2) to gate one of the lines mono-directionally, allowing signals to flow from the I^{2}C master device on

the multiplexer board to the slaves on the camera board but preventing signals from flowing in the reverse direction.

It would be impossible to gate the data line by this latter method as signals must flow in both directions. However, the only time a signal must propagate from slave to master along the clock line is when the master is transmitting a clock signal that is too fast for the slave to cope with. When this occurs the slave can hold the clock line low on each clock cycle to slow the clock down; the master must detect this and not start the next clock until the slave releases the line.

In the camera system, both relevant chips (SAA7191 and SAA7186) can accept an I^2C clock up to its maximum specified speed, so it was decided to use the PAL to provide a mono-directional gate on the I^2C clock line. This solution will also work with slower I^2C devices if the master's clock is sufficiently slow. The gating delay on the I^2C clock does not affect the working of the I^2C bus.

8. The backplane

The data transfer speed required over the backplane is 33–36 MHz. The original concept for the camera system was to have a bucket brigade backplane with D-type flip-flops between each camera board re-timing and passing the data down the line until they reached the multiplexer board at the far end of the line. Various designs of this nature were proposed, including a relatively inexpensive version which placed the flip-flops on the camera boards. However calculations showed that if the data were re-timed only at each transmitting camera board and on receipt at the multiplexer, tri-state drivers on a low cost 64-way ribbon cable backplane would allow standard 74F TTL to be used up to the maximum designed clock speed for the backplane of 36MHz, with up to sixteen camera boards arranged eight on either side of the multiplexer board (Figure 5).

The present system has eight camera boards, and operates reliably with the multiplexer board at the centre or either end of the backplane. Edges on the backplane are very clean with no ringing, and rise and fall times of approximately 10nS.

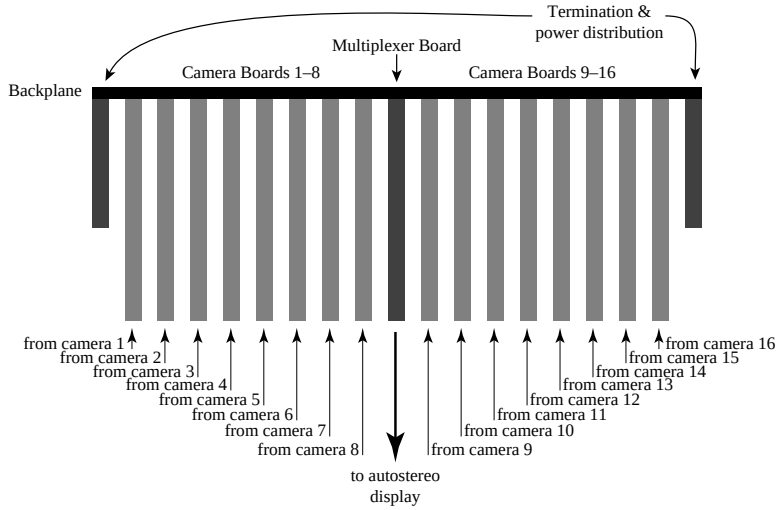

Figure 5: the maximum configuration of the autostereo camera system. Sixteen cameras' inputs are multiplexed into a single autostereoscopic video output. The backplane handles distribution of power, control and data. The two end circuit boards provide termination and power supply for the backplane.

The backplane consists of two 64-way 0.05" ribbon cables with DIN connectors spaced every 1.6". Each signal has an earthed (0 volt) line between it and the next signal. The nominal impedance of the ribbon pair is 100Ω. The repetitive loading of the cards every 1.6" decreases this to 75Ω, so a 75Ω termination is required at either end of the backplane. Each data and control line on the backplane is terminated at either end with 150Ω pull-up and pull-down resistors to +5 volts and ground (0 volts). This gives the necessary 75Ω termination, and gives a +2.5 volt minimum high logic level when the drive is open circuit. The maximum low current required from the backplane drivers is within the specification for 74F244 family gates. The I^2C data line is not terminated at all and has its own 2.2kΩ pull up resistor on the multiplexer board.

The termination resistors on the video data lines mean that, when the multiplexer accesses a camera board that is not present, the field from the

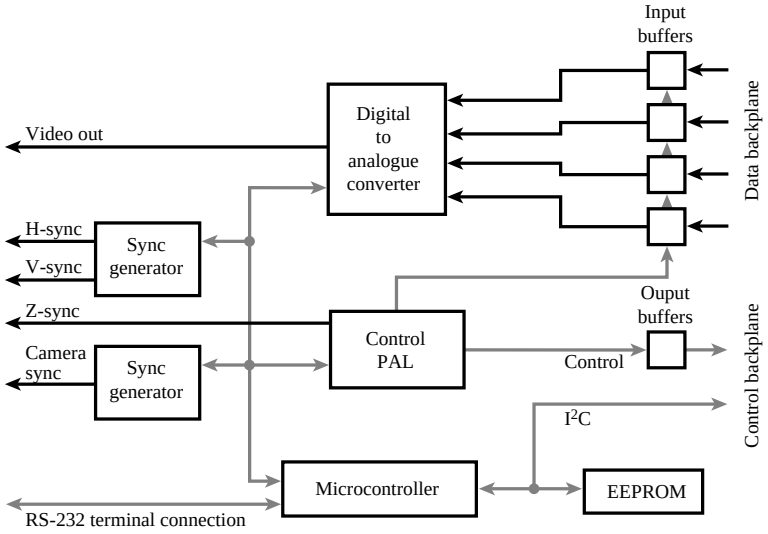

Figure 6: block diagram of the multiplexer board.

missing board will have all bits set to 1. In order that a missing board causes a black field to be displayed, the pixel data is inverted for transmission across the backplane. This inversion is performed by the SAA7186 and undone by the Bt458 D/A converter on the multiplexer board.

In addition to clock, data, and control signals, the backplane is used to distribute analogue power, digital power, and ground to multiplexer and camera boards. The power supply connectors and termination resistors are placed on two stub boards, one at either end of the backplane (Figure 5).

9. The multiplexer board

Figure 6 gives an overview of the multiplexer board. Video data is re-timed at the multiplexer board from the backplane via 32 D-type flip-flops. From these it flows directly into a Brooktree Bt458 4:1 multiplexed D/A converter. The monochrome analogue video output of the D/A is fed to the autostereo display through a 75Ω coaxial cable. The Bt458 operates at up to 165MHz output pixel rate, and is thus sufficiently fast for the current

autostereo display and the camera system's maximum design pixel rate of 144MHz.

The remainder of the multiplexer board contains circuitry to generate all the necessary control signals which drive the cameras, camera boards, and the autostereo display itself. Two National Semiconductor LM1882 programmable video sync generators provide video control signals for the camera array (composite sync at 50 or 60Hz field rate) and for the autostereo display (video blanking/active signal for the D/A and camera board output control; plus separate horizontal and vertical sync for the display itself, at up to 1200Hz field rate). The former sync generator also provides a pulse every field to which the rest of the circuitry is referenced. This ensures that the entire system is synchronised. While a composite sync signal could be generated for the autostereo display, separate horizontal and vertical sync signals are required by the PAL, and so these are generated instead.

This Mach-210 PAL controls the real time operation of the multiplexer. It is responsible for selecting which camera board is currently sending video data. It also generates the Z-sync signal, and it synchronises the two LM1882 sync generators when the micro-controller deems this necessary (usually on start-up or reset).

A Philips 87C654 micro-controller handles the programming of the Bt458, both LM1882s, and a register in the PAL on the multiplexer board. As master device on the I^2C bus it also programs all the SAA7191s and SAA7186s on the camera boards.

The I^2C bus also gives access to up to eight 256 byte EEPROM memory banks. Each bank holds a complete set of parameters for all programmable chips, and thus up to eight configurations are selectable at any one time.

The micro-controller is connected to the outside world through an RS-232 port. This enables on-line programming and debugging of the system using a custom program in the 87C654, whilst observing the image.

10. The synchronisation problem

The cameras supply an interlaced signal, and the autostereo display is configured to receive an interlaced signal. Alternate fields on the

autostereo display are odd and even, which means that the video stream to the display must consist of an odd field from camera one, followed by an even field from camera two, then odd three, even four, odd five, and so forth. With an even number of cameras, an extra blank field must be inserted at the end of the sequence of camera fields to ensure that alternate fields from each camera are displayed as odd and even on the autostereo display. This extra blank field has the added advantage that it attenuates any phosphor persistence between the final camera's image and the first camera's image, when the separation between the two images is a maximum.

The FIFOs on each camera board are loaded with field after field from the corresponding camera. At some point during each camera field the multiplexer board requests a field from each camera board. This field is read from the FIFOs onto the backplane an order of magnitude faster than it was written into the FIFOs, the FIFOs thus acting as a buffer. At any given time four fields are stored in the FIFOs. Each camera board's FIFOs are read reset and write reset by the multiplexer board. On any given camera field, alternate camera boards need to provide fields of alternating phase to the multiplexer board. This is achieved by resetting the FIFOs differently on the odd and even camera boards. FIFOs on all camera boards are reset for reading at every fourth field; FIFOs on odd boards are reset for writing one field later and, on even camera boards, two fields later than the read reset. This ensures correctly interlaced output to the autostereo display (Figure 7).

An alternate scheme would be to reset the FIFOs on all the boards simultaneously, and to synchronise the odd and even cameras separately. This was considered and rejected on the grounds that it required an extra sync generator and added unnecessary complexity in synchronising the sync generators to one another and in connecting the cameras correctly.

Extra flexibility has been added to the system by including logic in the Mach-110 PAL on the camera board to store the write reset signal from the multiplexer. This is only forwarded to the FIFOs once a complete field has been written to them, and before the next field starts. By doing this, the system can function adequately with cameras that cannot be synchronised.

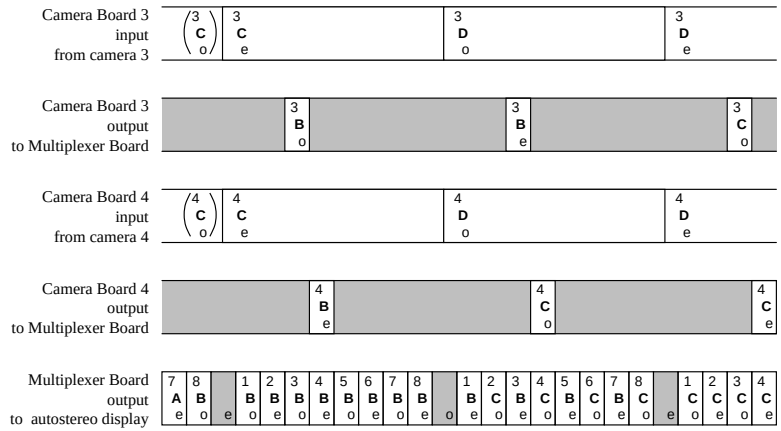

Figure 7: the input and output from the FIFOs on two camera boards and the output from the multiplexer board. Each field is labelled with the camera number, a frame identifier (**A**, **B**, **C**,…) and an indicator as to whether it is the odd (o) or even (e) field in that frame. Note that the even camera's output lags two fields behind its input, while the odd camera's output lags three fields behind its input, in order that the output fields are correctly synchronised with the interlacing of the autostereo display.

This is why the output from each camera board is designed to lag two and three fields behind the input, rather than simply one and two fields.

In this case however, odd and even fields may be sent to the autostereo display in the wrong phase (that is an odd field is sent when an even field is required, or vice versa). It also means that occasional fields may be dropped or repeated depending on whether a camera is running faster or slower (respectively) than the master sync generator on the multiplexer board.

A more complex program could be provided in the PAL on the camera board to prevent the odd/even mis-registration but, without global synchronisation of all cameras, nothing can be done to prevent the necessity of dropping or repeating fields.

11. 2D and 3D frame rates

To keep the cameras and autostereo display in precise synchronisation, exactly the same number of clock cycles are required for the input of a single 2D frame from the cameras as for the output of a multiplexed autostereo frame to the autostereo display. The basic formula for frame time, T_f, is:

$$F \times T_f = V_2 \times H_2 = N \times V_3 \times H_3$$

N is the number of views, V_2 and V_3 are the total number of scan lines in a pair of camera or autostereo display fields, and H_2 and H_3 are the number of clock cycles in a single scan line for camera and display respectively. F is the clock frequency.

There are constraints on these numbers. V_2 must be odd and close to 625 when 50 Hz PAL input is being used (V_2 would need to be near 525 for NTSC). H_3 is the sum of the time taken to display the video data for a single scan line, plus around 2.2µs fly back time. V_3 must take the 270µs vertical fly back into account and, overall, T_f must be close to 1/25s for PAL, or 1/30s for NTSC.

Taking PAL input from eight cameras and resizing the active picture area to 648 × 576 pixels, suitable values of the parameters are:

F = 144MHz

N = 9 (8 cameras + 1 blank)

V_2 = 627 (576 active + 51 fly back)

H_2 = 9240 (9240 at 144MHz = 946 pixels at PAL clock speed)

V_3 = 665 (576 active + 89 fly back)

H_3 = 968 (648 active + 320 fly back)

making T_f = 40.2325ms.

12. Power supply

The termination boards situated at either end of the backplane also supply analogue and digital TTL level power and ground to all boards on the backplane.

In addition, a 12V power supply is required to power the cameras. A separate circuit board is used in the prototype to distribute 12V power, ground, and the cameras' synchronisation signals via audio DIN connectors — one per camera. In a production system such distribution could be done very close to the cameras, minimising the number of actual wires required between the camera array and the control box, or it could be done from the camera boards themselves, thus requiring a simple 8–12 wire cable from each camera to its camera board.

All power required by the system is supplied to the termination and distribution boards by a commercial switching power supply connected to the mains supply.

13. Comparison with other systems

Many video multiplexes are currently in use, notably in video surveillance applications. Some, such as Sony's Sequential Switchers (YS-S104, YS-S6P) simply switch between cameras at intervals between one and sixty seconds. Panasonic's Digital Field Switcher (WJ-FS20) can switch between cameras on a field by field basis. In both cases input field rate and output field rate are the same. More akin to the present system are the Quad Units (e.g. Panasonic WJ-410, WJ-450; Sony YS-Q400P) which, while having the same input and output video rates, must combine four input streams to produce a single output stream. This involves the use of field buffers, the dropping of pixels from lines, and of lines from fields.

Many attempts have been made to produce camera systems for three dimensional displays. A variety of two-view stereoscopic camera systems have been developed [e.g. Lipt93, ScMD91, JoMM91]. Many simply produce a multiplexed output signal at twice the input field rate. Lipton [Lipt93] shows how this can be achieved without the need to increase the pixel rate by using half the usual lines per field, and a four fold interlace. Other systems tend to use either twice the standard pixel rate or a field sequential method, with one view on the odd, and one view on the even field.

[IYTK92] describe a four view camera system for use with a spatially-multiplexed lenticular display. The input and output pixel rates are the same, as are the frame rates. Each output field is pixel by pixel multiplexed

from the four source images. Every fourth pixel in each source image thus appears in the output.

While all these systems solve similar multiplexing problems as the autostereo camera system, the latter system is required to run an order of magnitude faster because it has to output all of its input data, rather than down-sampling it.

14. Future extensions

Having proven the system in monochrome, we aim to produce a modified multiplexer board to drive the six-view colour version of the autostereo display [MDTL96]. Research is also being undertaken in autostereo video recording. A further useful extension to the current system would be the ability to capture the autostereo image for processing on a computer.

This prototype system is costly. A commercial system could incorporate some, or all, of the following ideas:

- replace the FIFO field buffers with VRAM field buffers;
- move the field buffers from the camera boards to the multiplexer board, leaving only line buffers on the camera boards;
- use fewer circuit boards, for example use a single circuit board, or four camera digitisation circuits on a single board.

15. Summary

An autostereoscopic camera system has been designed and implemented. It is capable of taking video input from up to sixteen cameras, and multiplexing these into a video output stream with a pixel rate an order of magnitude faster than the individual input streams. Difficulties with both the Philips I^2C bus and the synchronisation of the video streams have been met and overcome. Testing of the system with eight cameras and a Cambridge Autostereo Display have produced excellent live autostereoscopic video. The next goal is the extension of this technology to the colour version of the display.

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